

3 Gbps HD/SD SDI Dual Output Cable Driver With Cable Detect

Check for Samples: [LMH0307](#)

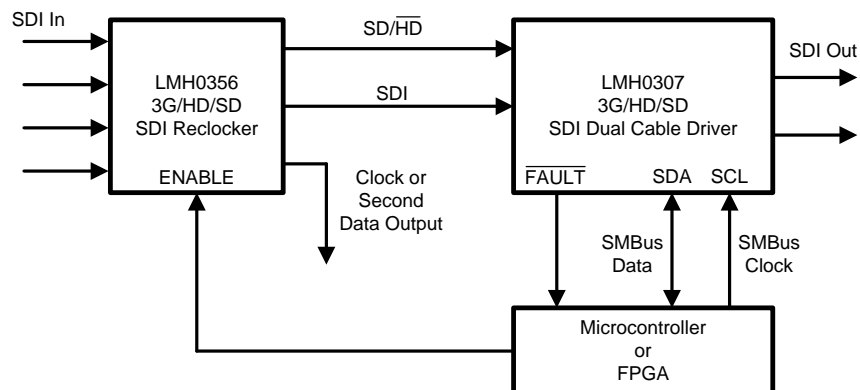
FEATURES

- **SMPTE 424M, SMPTE 292M, SMPTE 344M, and SMPTE 259M Compliant**
- **Data Rates to 2.97 Gbps**
- **Supports DVB-ASI at 270 Mbps**
- **Cable Detect on Output**
- **Loss of Signal Detect at Input**
- **Output Driver Power Down Control**
- **Typical Power Consumption: 230 mW in SD Mode and 275 mW in HD Mode**
- **Power Save Mode Typical Power Consumption: 4 mW**
- **Single 3.3V Supply Operation**
- **Differential Input**
- **Dual Complementary 75Ω Outputs**
- **Selectable Slew Rate**
- **Industrial Temperature Range: –40°C to +85°C**
- **16-Pin WQFN or 25-Ball CS-BGA package**

APPLICATIONS

- **SMPTE 424M, SMPTE 292M, SMPTE 344M, and SMPTE 259M Serial Digital Interfaces**
- **Digital Video Routers and Switches**
- **Distribution Amplifiers**

Typical Application



DESCRIPTION

The LMH0307 3 Gbps HD/SD SDI Dual Output Cable Driver with Cable Detect is designed for use in SMPTE 424M, SMPTE 292M, SMPTE 344M, and SMPTE 259M serial digital video applications. The LMH0307 implements two complementary output drivers and drives 75Ω transmission lines (Belden 1694A, Belden 8281, or equivalent) at data rates up to 2.97 Gbps.

The LMH0307 includes intelligent sensing capabilities to improve system diagnostics. The cable detect feature senses near-end termination to determine if a cable is correctly attached to the output BNC. Input loss of signal (LOS) detects the presence of a valid signal at the input of the cable driver. These sensing features may be used to alert the user of a system fault and activate a deep power save mode, reducing the cable driver's power consumption to 4 mW. These features are accessible via an SMBus interface.

The LMH0307 provides two selectable slew rates for SMPTE 259M and SMPTE 424M / 292M compliance. The output amplitude is adjustable ±10% in 5 mV steps via the SMBus.

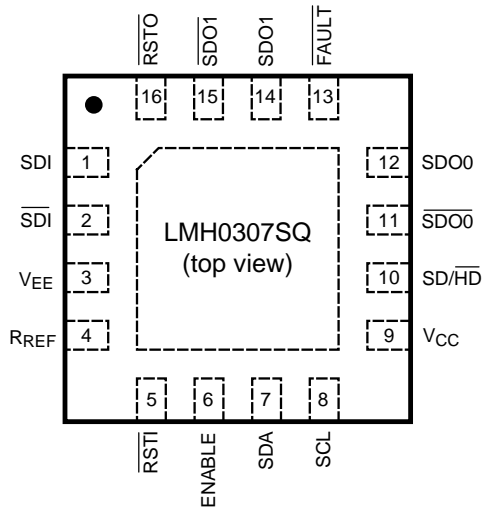
The LMH0307 is powered from a single 3.3V supply. Power consumption is typically 230 mW in SD mode and 275 mW in HD mode. The LMH0307 is available in two space-saving packages: a 4 x 4 mm 16-pin WQFN and even more space-efficient 3 x 3 mm 25-ball CS-BGA package.



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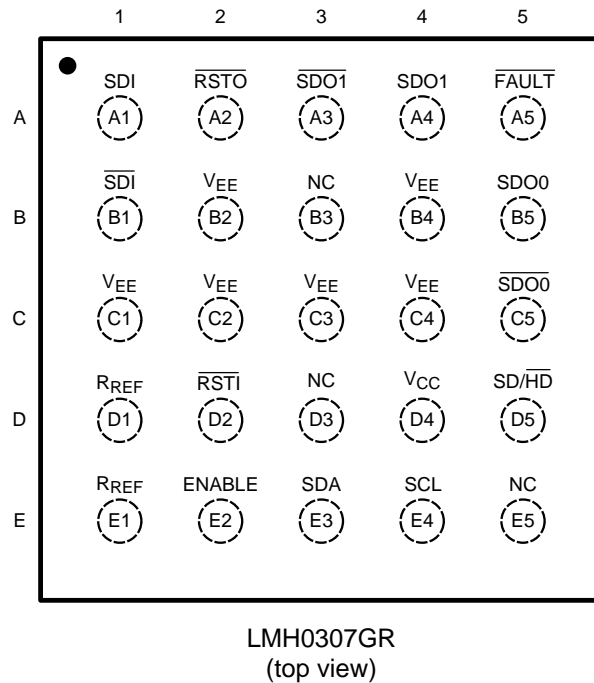
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Connection Diagram



The exposed die attach pad is a negative electrical terminal for this device. It should be connected to the negative power supply voltage.

Figure 1. 16-Pin WQFN Package Number RUM



LMH0307GR
(top view)

Figure 2. 25-Ball CS-BGA Package Number NYA

PIN DESCRIPTIONS

| WQFN Pin | CS-BGA Ball | Name | Description |
|----------|------------------------|----------------------------|--|
| 1 | A1 | SDI | Serial data true input. |
| 2 | B1 | $\overline{\text{SDI}}$ | Serial data complement input. |
| 4 | D1, E1 | R _{REF} | Bias resistor. Connect a 750Ω resistor to V _{CC} (also connect D1 to E1 on CS-BGA version). |
| 5 | D2 | $\overline{\text{RSTI}}$ | Reset input. $\overline{\text{RSTI}}$ has an internal pullup. H = Normal operation. L = Device reset. The device operates with default register settings. Forcing $\overline{\text{RSTI}}$ low also forces $\overline{\text{RSTO}}$ low. |
| 6 | E2 | ENABLE | Output driver enable. ENABLE has an internal pullup. H = Normal operation. L = Output driver powered off. |
| 7 | E3 | SDA | SMBus bidirectional data pin. When functioning as an output, it is open drain. This pin requires an external pullup. |
| 8 | E4 | SCL | SMBus clock input. SCL is input only. This pin requires an external pullup. |
| 10 | D5 | SD/ $\overline{\text{HD}}$ | Output slew rate control. SD/ $\overline{\text{HD}}$ has an internal pulldown. H = Output rise/fall time complies with SMPTE 259M. L = Output rise/fall time complies with SMPTE 424M / 292M. |
| 11 | C5 | $\overline{\text{SDO0}}$ | Serial data output 0 complement output. |
| 12 | B5 | SDO0 | Serial data output 0 true output. |
| 13 | A5 | $\overline{\text{FAULT}}$ | Fault open drain output flag. Requires external pullup resistor and may be wire ORed with multiple cable drivers. H = Normal operation. L = Loss of signal or termination fault for any output. |
| 14 | A4 | SDO1 | Serial data output 1 true output. |
| 15 | A3 | $\overline{\text{SDO1}}$ | Serial data output 1 complement output. |
| 16 | A2 | $\overline{\text{RSTO}}$ | Reset output. $\overline{\text{RSTO}}$ is automatically set to 1 when register 0 is written. It can be reset back to zero by forcing $\overline{\text{RSTI}}$ to zero to reset the device. Used to daisy chain multiple cable drivers on the same SMBus. |
| 9 | D4 | V _{CC} | Positive power supply (+3.3V). |
| DAP, 3 | B2, B4, C1, C2, C3, C4 | V _{EE} | Negative power supply (ground). |
| — | B3, D3, E5 | NC | No connect. |



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾

| | | |
|------------------------------------|------------------------------|------------------------|
| Supply Voltage | | -0.5V to 3.6V |
| Input Voltage (all inputs) | | -0.3V to $V_{CC}+0.3V$ |
| Output Current | | 28 mA |
| Storage Temperature Range | | -65°C to +150°C |
| Junction Temperature | | +125°C |
| Lead Temperature (Soldering 4 Sec) | | +260°C |
| Package Thermal Resistance | θ_{JA} 16-pin WQFN | +43°C/W |
| | θ_{JC} 16-pin WQFN | +7°C/W |
| | θ_{JA} 25-ball CS-BGA | +67.6°C/W |
| ESD Rating | HBM | 8 kV |
| | MM | 400V |
| | CDM | 2 kV |

- (1) "Absolute Maximum Ratings" are those parameter values beyond which the life and operation of the device cannot be ensured. The stating herein of these maximums shall not be construed to imply that the device can or should be operated at or beyond these values. The table of [Electrical Characteristics](#) specifies acceptable device operating conditions.

Recommended Operating Conditions

| | |
|--|----------------|
| Supply Voltage ($V_{CC} - V_{EE}$) | 3.3V $\pm 5\%$ |
| Operating Free Air Temperature (T_A) | -40°C to +85°C |

DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified⁽¹⁾⁽²⁾.

| Symbol | Parameter | Conditions | Reference | Min | Typ | Max | Units |
|--------------------------------|---|---|--|------------------------------|---------------------------------------|--|-------------------|
| V _{CMIN} | Input Common Mode Voltage | | SDI, $\overline{\text{SDI}}$ | 1.6 + V _{SDI} /2 | | V _{CC} – V _{SDI} /2 | V |
| V _{SDI} | Input Voltage Swing | Differential | | 100 | | 2200 | mV _{P-P} |
| V _{CMOUT} | Output Common Mode Voltage | | SDO, $\overline{\text{SDO}}$ | | V _{CC} – V _{SDO} | | V |
| V _{SDO} | Output Voltage Swing | Single-ended, 75Ω load, R _{REF} = 750Ω 1% | | 720 | 800 | 880 | mV _{P-P} |
| V _{IH} | Input Voltage High Level | | SD/ $\overline{\text{HD}}$, ENABLE | 2.0 | | | V |
| V _{IL} | Input Voltage Low Level | | | | | 0.8 | V |
| I _{CC} | Supply Current | SD/ $\overline{\text{HD}}$ = 0, SDO/ $\overline{\text{SDO}}$ enabled | | | 84 | 100 | mA |
| | | SD/ $\overline{\text{HD}}$ = 1, SDO/ $\overline{\text{SDO}}$ enabled | | | 70 | 77 | mA |
| | | SDO/ $\overline{\text{SDO}}$ disabled | | | 1.3 | 2.5 | mA |
| SMBus DC Specifications | | | | | | | |
| V _{SIL} | Data, Clock Input Low Voltage | | | | | 0.8 | V |
| V _{SIH} | Data, Clock Input High Voltage | | | 2.1 | | V _{SDD} | V |
| I _{SPULLUP} | Current through pullup resistor or current source | V _{OL} = 0.4V | | 4 | | | mA |
| V _{SDD} | Nominal Bus Voltage | | | 3.0 | | 3.6 | V |
| I _{SLEAKB} | Input Leakage per bus segment | (3) | | –200 | | 200 | μA |
| I _{SLEAKP} | Input Leakage per pin | | | –10 | | 10 | μA |
| C _{SI} | Capacitance for SDA and SCL | (3)(4) | | | | 10 | pF |

(1) Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to V_{EE} = 0 Volts.

(2) Typical values are stated for V_{CC} = +3.3V and T_A = +25°C.

(3) Recommended value — Parameter not tested.

(4) Recommended maximum capacitive load per bus segment is 400 pF.

AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified⁽¹⁾.

| Symbol | Parameter | Conditions | Reference | Min | Typ | Max | Units |
|---------------------------------|-----------------------------|---|------------------------------|-----|-----|------|-------|
| DR _{SDI} | Input Data Rate | | SDI, $\overline{\text{SDI}}$ | | | 2970 | Mbps |
| t _{jit} | Additive Jitter | 2.97 Gbps | SDO, $\overline{\text{SDO}}$ | | 20 | | pSp-p |
| | | 1.485 Gbps | | | 18 | | pSp-p |
| | | 270 Mbps | | | 15 | | pSp-p |
| t _r , t _f | Output Rise Time, Fall Time | SD/ $\overline{\text{HD}}$ = 0, 20% – 80%, SD/ $\overline{\text{HD}}$ = 1, 20% – 80% | | | 90 | 130 | ps |
| | | | | 400 | | 800 | ps |
| | Mismatch in Rise/Fall Time | SD/ $\overline{\text{HD}}$ = 0 | | | | 30 | ps |
| | | SD/ $\overline{\text{HD}}$ = 1 | | | | 50 | ps |
| | Duty Cycle Distortion | SD/ $\overline{\text{HD}}$ = 0, 2.97 Gbps ⁽²⁾ | | | | 27 | ps |
| | | SD/ $\overline{\text{HD}}$ = 0, 1.485 Gbps ⁽²⁾ | | | | 30 | ps |
| | | SD/ $\overline{\text{HD}}$ = 1 ⁽²⁾ | | | | 100 | ps |
| t _{OS} | Output Overshoot | SD/ $\overline{\text{HD}}$ = 0 ⁽²⁾ | | | | 10 | % |
| | | SD/ $\overline{\text{HD}}$ = 1 ⁽²⁾ | | | | 8 | % |
| t _{SK} | SDO1 to SDO0 Skew | SD/ $\overline{\text{HD}}$ = 0 ⁽²⁾ | | | | 8 | ps |
| | | SD/ $\overline{\text{HD}}$ = 1 ⁽²⁾ | | | | 54 | ps |
| RL _{SDO} | Output Return Loss | 5 MHz - 1.5 GHz ⁽³⁾ | | 15 | | | dB |
| | | 1.5 GHz - 3.0 GHz ⁽³⁾ | | 10 | | | dB |

SMBus AC Specifications

| | | | | | | | |
|---------------------|--|-------------------------------|--|-----|--|------|-----|
| f _{SMB} | Bus Operating Frequency | | | 10 | | 100 | kHz |
| t _{BUF} | Bus free time between Stop and Start Condition | | | 4.7 | | | μs |
| t _{HD:STA} | Hold time after (repeated) Start Condition. After this period, the first clock is generated. | At I _{SPULLUP} = MAX | | 4.0 | | | μs |
| t _{SU:STA} | Repeated Start Condition setup time | | | 4.7 | | | μs |
| t _{SU:STO} | Stop Condition setup time | | | 4.0 | | | μs |
| t _{HD:DAT} | Data hold time | | | 300 | | | ns |
| t _{SU:DAT} | Data setup time | | | 250 | | | ns |
| t _{LOW} | Clock low period | | | 4.7 | | | μs |
| t _{HIGH} | Clock high period | | | 4.0 | | 50 | μs |
| t _F | Clock/Data Fall Time | | | | | 300 | ns |
| t _R | Clock/Data Rise Time | | | | | 1000 | ns |
| t _{POR} | Time in which device must be operational after power on | | | | | 500 | ms |

(1) Typical values are stated for V_{CC} = +3.3V and T_A = +25°C.

(2) Specification is ensured by characterization.

(3) Output return loss is dependent on board design. The LMH0307 meets this specification on the SD307 evaluation board.

TIMING DIAGRAM

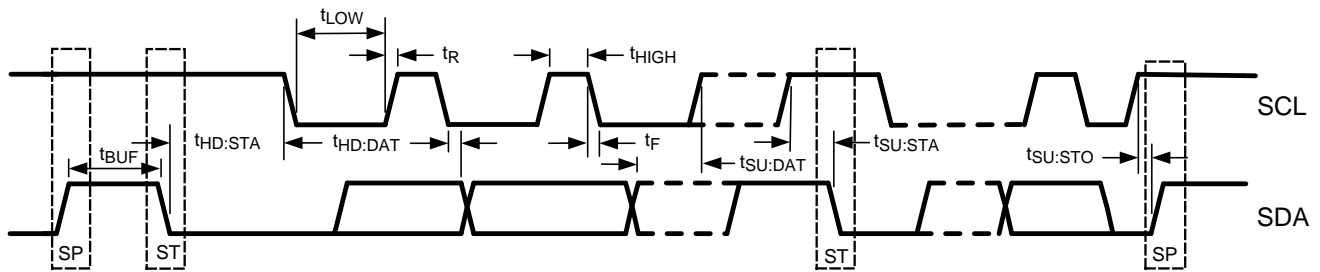


Figure 3. SMBus Timing Parameters

DEVICE OPERATION

INPUT INTERFACING

The LMH0307 accepts either differential or single-ended input. For single-ended operation, the unused input must be properly terminated.

OUTPUT INTERFACING

The LMH0307 uses current mode outputs. Single-ended output levels are 800 mV_{P-P} into 75Ω AC-coupled coaxial cable with an R_{REF} resistor of 750Ω. The R_{REF} resistor is connected between the R_{REF} pin and V_{CC}. The only resistor value that should be used for R_{REF} is 750Ω.

The R_{REF} resistor should be placed as close as possible to the R_{REF} pin. In addition, the copper in the plane layers below the R_{REF} network should be removed to minimize parasitic capacitance.

OUTPUT SLEW RATE CONTROL

The LMH0307 output rise and fall times are selectable for either SMPTE 259M or SMPTE 424M / 292M compliance via the SD/HD pin. For slower rise and fall times, or SMPTE 259M compliance, SD/HD is set high. For faster rise and fall times, or SMPTE 424M and SMPTE 292M compliance, SD/HD is set low. SD/HD may also be controlled using the SMBus, provided the SD/HD pin is held low. SD/HD has an internal pulldown.

OUTPUT ENABLE

The SDO0/SDO0 and SDO1/SDO1 output drivers can be enabled or disabled with the ENABLE pin. When set low, both output drivers are powered off and the LMH0307 enters a deep power save mode. ENABLE has an internal pullup.

INPUT LOSS OF SIGNAL DETECTION (LOS)

The LMH0307 detects when the input signal does not have a video-like pattern. Self oscillation and low levels of noise are rejected. This loss of signal detect allows a very sensitive input stage that is robust against coupled noise without any degradation of jitter performance.

Via the SMBus, the loss of signal detect can either add an input offset or mute the outputs. An offset is added by default. Additionally, the loss of signal detect can be linked to the ENABLE functionality so that when the LOS goes low, ENABLE will also go low.

OUTPUT CABLE DETECTION

The LMH0307 detects when an output is locally terminated. When a video signal (or AC test signal) is present on SDI, the device senses the SDO and SDO amplitudes. If the output is not properly terminated (via a terminated cable or local termination), the amplitude will be higher than expected, and the Termination Fault signal is asserted. The Termination Fault signal is de-asserted when the proper termination is applied. This feature allows the system designer the flexibility to react to cable attachment and removal. Note that a long length of cable will look like a proper termination at the device output.

The cable driver must be enabled for the termination detection to operate. If the Termination Fault will be used to power down the LMH0307, then periodic polling (enabling) is recommended to monitor the output termination. For example, when a Fault condition is triggered, ENABLE can be driven low to power down the device. The LMH0307 should be re-enabled periodically to check the status of the output termination. The LMH0307 needs to be powered on for roughly 4 ms for Termination Fault detection to work.

SMBUS INTERFACE

The System Management Bus (SMBus) is a two-wire interface designed for the communication between various system component chips. By accessing the control functions of the circuit via the SMBus, pin count is kept to a minimum while allowing a maximum amount of versatility. The LMH0307 has several internal configuration registers which may be accessed via the SMBus.

The 7-bit default address for the LMH0307 is 17h. The LSB is set to 0b for a WRITE and 1b for a READ, so the 8-bit default address for a WRITE is 2Eh and the 8-bit default address for a READ is 2Fh. The SMBus address may be dynamically changed.

In applications where there might be several LMH0307s, the SDA, SCL, and $\overline{\text{FAULT}}$ pins can be shared. The SCL, SDA, and $\overline{\text{FAULT}}$ pins are open drain and require external pullup resistors. Multiple LMH0307s may have the $\overline{\text{FAULT}}$ pin wire ORed. This signal becomes active when either loss of signal is detected or any termination faults are detected. The registers may be read in order to determine the cause. Additionally, each signal can be masked from the $\overline{\text{FAULT}}$ pin.

TRANSFER OF DATA VIA THE SMBus

During normal operation the data on SDA must be stable during the time when SCL is High.

There are three unique states for the SMBus:

START: A High-to-Low transition on SDA while SCL is High indicates a message START condition.

STOP: A Low-to-High transition on SDA while SCL is High indicates a message STOP condition.

IDLE: If SCL and SDA are both High for a time exceeding t_{BUF} from the last detected STOP condition or if they are High for a total exceeding the maximum specification for t_{HIGH} then the bus will transfer to the IDLE state.

SMBus TRANSACTIONS

The device supports WRITE and READ transactions. See [Table 1](#) for register address, type (Read/Write, Read Only), default value and function information.

WRITING A REGISTER

To write a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a "0" indicating a WRITE.
2. The Device (Slave) drives the ACK bit ("0").
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit ("0").
5. The Host drives the 8-bit data byte.
6. The Device drives an ACK bit ("0").
7. The Host drives a STOP condition.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

READING A REGISTER

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drives a START condition.
6. The Host drives the 7-bit SMBus Address, and a “1” indicating a READ.
7. The Device drives an ACK bit “0”.
8. The Device drives the 8-bit data value (register contents).
9. The Host drives a NACK bit “1” indicating end of the READ transfer.
10. The Host drives a STOP condition.

APPLICATION INFORMATION

Figure 4 shows the application circuit for the LMH0307.

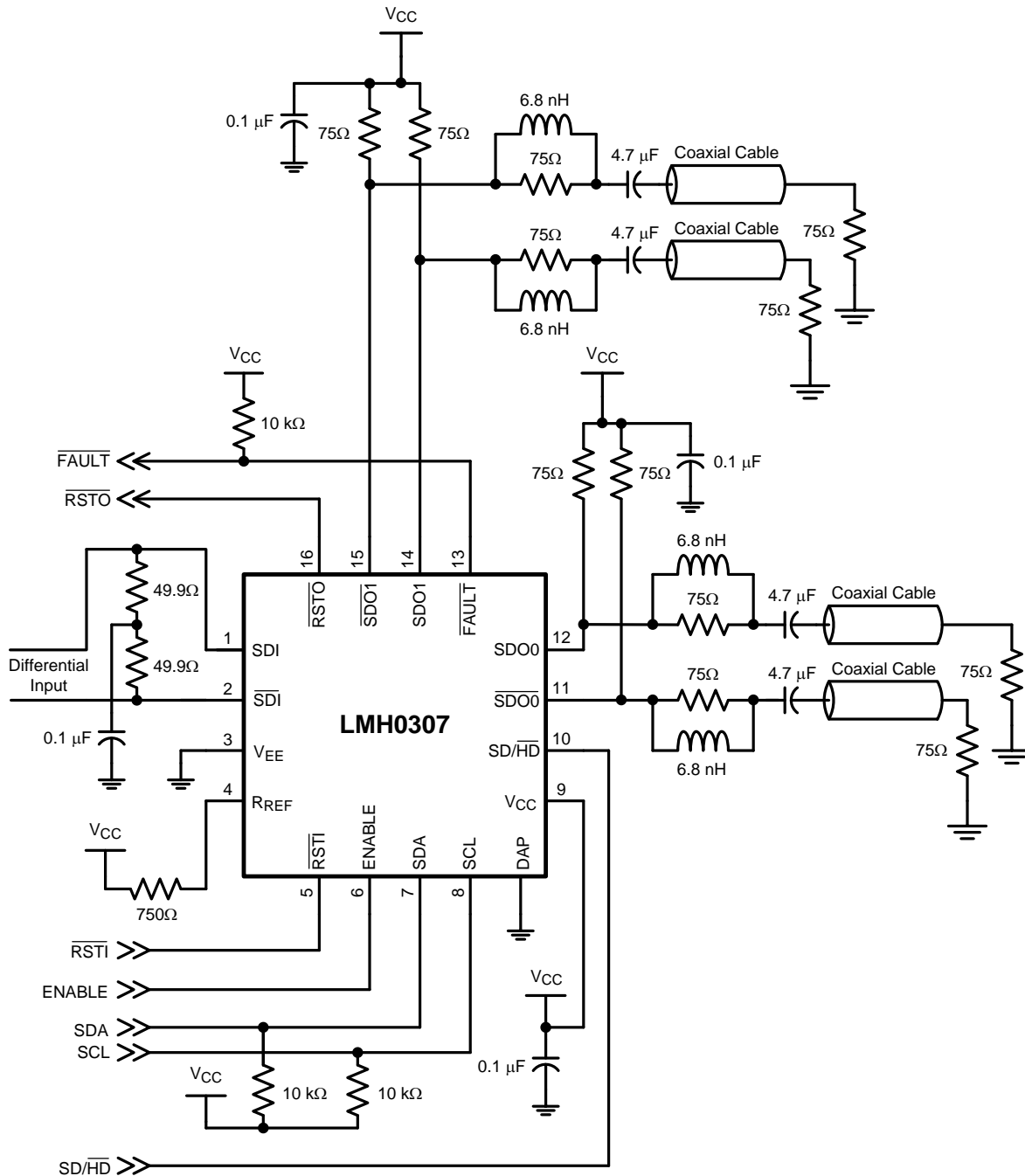


Figure 4. Application Circuit

COMMUNICATING WITH MULTIPLE LMH0307 CABLE DRIVERS VIA THE SMBus

A common application for the LMH0307 will utilize multiple cable driver devices. Even though the LMH0307 devices all have the same default SMBus device ID (address), it is still possible for them share the SMBus signals as shown in Figure 5. A third signal is required from the host to the first device. This signal acts as a "Enable / Reset" signal. Additional LMH0307s are controlled from the upstream device. In this control scheme, multiple LMH0307s may be controlled via the two-wire SMBus and the use of one GPO (General Purpose Output) signal. Other SMBus devices may also be connected to the two wires, assuming they have their own unique SMBus addresses.

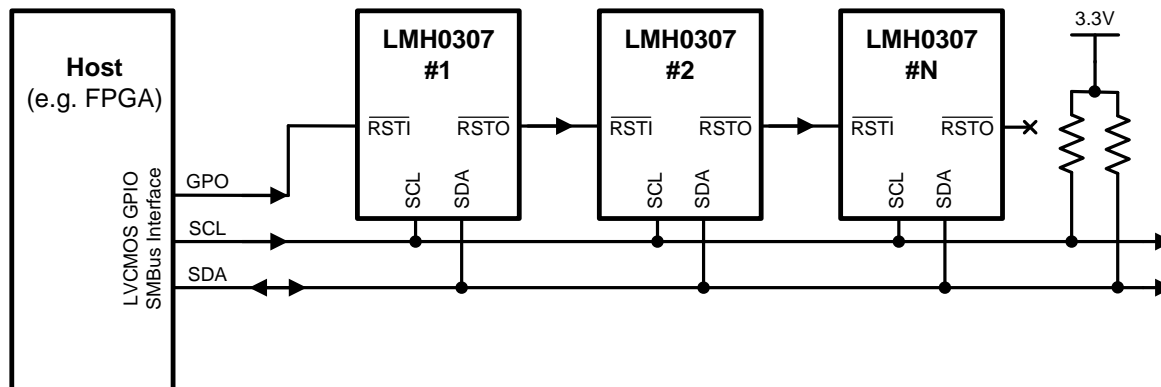


Figure 5. SMBus Configuration for Multiple LMH0307 Cable Drivers

The $\overline{\text{RSTI}}$ pin of the first device is controlled by the system with a GPO pin from the host. The first LMH0307 $\overline{\text{RSTO}}$ pin is then daisy chained to the next device's $\overline{\text{RSTI}}$ pin. That device's $\overline{\text{RSTO}}$ pin is connected to the next device and so on.

The procedure at initialization is to:

1. Hold the host GPO pin Low in RESET, to the first device. $\overline{\text{RSTO}}$ output default is also Low which holds the next device in RESET in the chain.
2. Raise the host GPO signal to LMH0307 #1 $\overline{\text{RSTI}}$ input pin.
3. Write to Address 8'h2E (7'h17) Register 0 with the new address value (e.g. 8'h2C (7'h16)).
4. Upon writing Register 0 in LMH0307 #1, its $\overline{\text{RSTO}}$ signal will switch High. Its new address is 8'h2C (7'h16), and the next LMH0307 in the chain will now respond to the default address of 8'h2E (7'h17).
5. The process is repeated until all LMH0307 devices have a unique address loaded.
6. Direct SMBus writes and reads may now take place between the host and any addressed device.

The 7-bit address field allows for 128 unique addresses. The above procedure allows for the reprogramming of the LMH0307 devices such that multiple devices may share the two-wire SMBus. Make sure all devices on the bus have unique device IDs.

If power is toggled to the system, the SMBus address routine needs to be repeated.

Table 1. SMBus Registers

| Address | R/W | Name | Bits | Field | Default | Description |
|---------|-----|--------|------|-------|---------|---|
| 00h | R/W | ID | 7:1 | DEVID | 0010111 | Device ID. Writing this register will force the RSTO pin high. Further accesses to the device must use this 7-bit address. |
| | | | 0 | RSVD | 0 | Reserved as 0. Always write 0 to this bit. |
| 01h | R | STATUS | 7:5 | RSVD | 000 | Reserved. |
| | | | 4 | TF1N | 0 | Termination Fault for $\overline{\text{SDI1}}$. 0: No Termination Fault Detected. 1: Termination Fault Detected. |
| | | | 3 | TF1P | 0 | Termination Fault for SDI1 . 0: No Termination Fault Detected. 1: Termination Fault Detected. |
| | | | 2 | TF0N | 0 | Termination Fault for $\overline{\text{SDI0}}$. 0: No Termination Fault Detected. 1: Termination Fault Detected. |
| | | | 1 | TF0P | 0 | Termination Fault for SDI0 . 0: No Termination Fault Detected. 1: Termination Fault Detected. |
| | | | 0 | LOS | 0 | Loss Of Signal ($\overline{\text{LOS}}$) detect at input. 0: No Signal Detected. 1: Signal Detected. |
| 02h | R/W | MASK | 7 | SD | 0 | SD Rate select bit. If the $\overline{\text{SD/HD}}$ pin is set to V_{CC} , it overrides this bit. With the $\overline{\text{SD/HD}}$ pin set to ground, this bit selects the output edge rate as follows: 0: HD edge rate. 1: SD edge rate. |
| | | | 6 | PD1 | 0 | Power Down for SDO1 output stage. If the ENABLE pin is set to ground, it overrides this bit. With the ENABLE pin set to V_{CC} , PD1 functions as follows: 0: SDO1 active. 1: SDO1 powered down. |
| | | | 5 | PD0 | 0 | Power Down for SDO0 output stage. If the ENABLE pin is set to ground, it overrides this bit. With the ENABLE pin set to V_{CC} , PD0 functions as follows: 0: SDO0 active. 1: SDO0 powered down. |
| | | | 4 | MTF1N | 0 | Mask TF1N from affecting $\overline{\text{FAULT}}$ pin. 0: TF1N=1 will cause $\overline{\text{FAULT}}$ to be 0. 1: TF1N=1 will not affect $\overline{\text{FAULT}}$; the condition is masked off. |
| | | | 3 | MTF1P | 0 | Mask TF1P from affecting $\overline{\text{FAULT}}$ pin. 0: TF1P=1 will cause $\overline{\text{FAULT}}$ to be 0. 1: TF1P=1 will not affect $\overline{\text{FAULT}}$; the condition is masked off. |
| | | | 2 | MTF0N | 0 | Mask TF0N from affecting $\overline{\text{FAULT}}$ pin. 0: TF0N=1 will cause $\overline{\text{FAULT}}$ to be 0. 1: TF0N=1 will not affect $\overline{\text{FAULT}}$; the condition is masked off. |
| | | | 1 | MTF0P | 0 | Mask TF0P from affecting $\overline{\text{FAULT}}$ pin. 0: TF0P=1 will cause $\overline{\text{FAULT}}$ to be 0. 1: TF0P=1 will not affect $\overline{\text{FAULT}}$; the condition is masked off. |
| | | | 0 | MLOS | 0 | Mask $\overline{\text{LOS}}$ from affecting $\overline{\text{FAULT}}$ pin. 0: $\overline{\text{LOS}}=0$ will cause $\overline{\text{FAULT}}$ to be 0. 1: $\overline{\text{LOS}}=0$ will not affect $\overline{\text{FAULT}}$; the condition is masked off. |

Table 1. SMBus Registers (continued)

| Address | R/W | Name | Bits | Field | Default | Description |
|---------|-----|-----------|------|----------------|---------|--|
| 03h | R/W | DIRECTION | 7 | HDTF0ThreshLSB | 1 | Least Significant Bit for HDTF0Thresh detection threshold. Combines with HDTF0Thresh bits in register 04h. |
| | | | 6 | SDTF0ThreshLSB | 1 | Least Significant Bit for SDTF0Thresh detection threshold. Combines with SDTF0Thresh bits in register 05h. |
| | | | 5 | RSVD | 0 | Reserved as 0. Always write 0 to this bit. |
| | | | 4 | DTF1N | 0 | Direction of TF1N that affects $\overline{\text{FAULT}}$ pin (when not masked). 0: TF1N=1 will cause $\overline{\text{FAULT}}$ to be 0 (when the condition is not masked off). 1: TF1N=0 will cause $\overline{\text{FAULT}}$ to be 0 (when the condition is not masked off). |
| | | | 3 | DTF1P | 0 | Direction of TF1P that affects $\overline{\text{FAULT}}$ pin (when not masked). 0: TF1P=1 will cause $\overline{\text{FAULT}}$ to be 0 (when the condition is not masked off). 1: TF1P=0 will cause $\overline{\text{FAULT}}$ to be 0 (when the condition is not masked off). |
| | | | 2 | DTF0N | 0 | Direction of TF0N that affects $\overline{\text{FAULT}}$ pin (when not masked). 0: TF0N=1 will cause $\overline{\text{FAULT}}$ to be 0 (when the condition is not masked off). 1: TF0N=0 will cause $\overline{\text{FAULT}}$ to be 0 (when the condition is not masked off). |
| | | | 1 | DTF0P | 0 | Direction of TF0P that affects $\overline{\text{FAULT}}$ pin (when not masked). 0: TF0P=1 will cause $\overline{\text{FAULT}}$ to be 0 (when the condition is not masked off). 1: TF0P=0 will cause $\overline{\text{FAULT}}$ to be 0 (when the condition is not masked off). |
| | | | 0 | DLOS | 0 | Direction of $\overline{\text{LOS}}$ that affects $\overline{\text{FAULT}}$ pin (when not masked). 0: LOS=0 will cause $\overline{\text{FAULT}}$ to be 0 (when the condition is not masked off). 1: LOS=1 will cause $\overline{\text{FAULT}}$ to be 0 (when the condition is not masked off). |
| 04h | R/W | OUTPUT0 | 7:5 | HDTF0Thresh | 100 | Sets the Termination Fault threshold for SDO0, when SD is set to HD rates (0). Combines with HDTF0ThreshLSB in register 03h (default for combined value is 1001). |
| | | | 4:0 | AMP0 | 10000 | SDO0 output amplitude in roughly 5 mV steps. |

Table 1. SMBus Registers (continued)

| Address | R/W | Name | Bits | Field | Default | Description |
|---------|-----|-------------|------|----------------|---------|---|
| 05h | R/W | OUTPUT0CTRL | 7 | RSVD | 0 | Reserved as 0. Always write 0 to this bit. |
| | | | 6 | FLOSOFF | 0 | Force $\overline{\text{LOS}}$ to always OFF in regard to its effect on the output signal. This forces the device into either the mute or “add offset” state. The $\overline{\text{LOS}}$ bit in register 01h still reflects the correct state of $\overline{\text{LOS}}$. 0: $\overline{\text{LOS}}$ operates normally, muting or adding offset as specified by the MUTE bit. 1: Muting or adding offset is always in place as specified by the MUTE bit. |
| | | | 5 | FLOSON | 0 | Force $\overline{\text{LOS}}$ to always ON in regard to its effect on the output signal. This prevents the device from muting or adding offset. The $\overline{\text{LOS}}$ bit in register 01h still reflects the correct state of $\overline{\text{LOS}}$. 0: $\overline{\text{LOS}}$ operates normally, muting or adding offset as specified in the MUTE bit. 1: Muting or adding offset never occurs. |
| | | | 4 | LOSEN | 0 | Configures $\overline{\text{LOS}}$ to be combined with the ENABLE functionality. 0: Only the PD bits and ENABLE pin affect the power down state of the output drivers. 1: If the ENABLE pin is set to ground, it powers down the output drivers regardless of the state of $\overline{\text{LOS}}$ or the PD bits. With the ENABLE pin set to V_{CC} , $\overline{\text{LOS}}=0$ will power down the output drivers, and $\overline{\text{LOS}}=1$ will leave the power down state dependent on the PD bits. |
| | | | 3 | MUTE | 0 | Selects whether the device will MUTE when loss of signal is detected or add an offset to prevent self oscillation. When an input signal is detected ($\overline{\text{LOS}}=1$), the device will operate normally. 0: Loss of signal will force a small offset to prevent self oscillation. 1: Loss of signal will force the channel to MUTE. |
| | | | 2:0 | SDTF0Thresh | 010 | Sets the Termination Fault threshold for SDO0, when SD is set to SD rates (1). Combines with SDTF0ThreshLSB in register 03h (default for combined value is 0101). |
| 06h | R/W | OUTPUT1 | 7:5 | HDTF1Thresh | 100 | Sets the Termination Fault threshold for SDO1, when SD is set to HD rates (0). Combines with HDTF1ThreshLSB in register 07h (default for combined value is 1001). |
| | | | 4:0 | AMP1 | 10000 | SDO1 output amplitude in roughly 5 mV steps. |
| 07h | R/W | OUTPUT1CTRL | 7 | HDTF1ThreshLSB | 1 | Least Significant Bit for HDTF1Thresh detection threshold. Combines with HDTF1Thresh bits in register 06h. |
| | | | 6 | SDTF1ThreshLSB | 1 | Least Significant Bit for SDTF1Thresh detection threshold. Combines with SDTF1Thresh bits in register 07h. |
| | | | 5:3 | RSVD | 011 | Reserved as 011. Always write 011 to these bits. |
| | | | 2:0 | SDTF1Thresh | 010 | Sets the Termination Fault threshold for SDO1, when SD is set to SD rates (1). Combines with SDTF1ThreshLSB in bit 6 (default for combined value is 0101). |

Table 1. SMBus Registers (continued)

| Address | R/W | Name | Bits | Field | Default | Description |
|---------|-----|-----------|------|-----------|---------|--|
| 08h | R/W | TEST | 7:5 | CMPCMD | 000 | Compare command. Determines whether the peak value or the current value of the Termination Fault counters is read in registers 0Ah-0Dh. 000: Resets compare value to 00; registers 0Ah-0Dh all show current counter values. Sets detection to look for MAX peak values. 001: Capture counter 0. Register 0Ah shows peak value. 010: Capture counter 1. Register 0Bh shows peak value. 011: Capture counter 2. Register 0Ch shows peak value. 100: Capture counter 3. Register 0Dh shows peak value. 101: Resets compare value to 1Fh. Sets detection to look for MIN peak values. 110, 111: Reserved. |
| | | | 4:0 | RSVD | 00000 | Reserved as 00000. Always write 00000 to these bits. |
| 09h | R | REV | 7:5 | RSVD | 000 | Reserved. |
| | | | 4:3 | DIEREV | 10 | Die Revision. |
| | | | 2:0 | PARTID | 010 | Part Identifier. Note that single output devices (LMH0303) have the LSB=1. Dual output devices (LMH0307) have the LSB=0. |
| 0Ah | R | TF0PCOUNT | 7:5 | RSVD | 000 | Reserved. |
| | | | 4:0 | TF0PCOUNT | 00000 | This is either the current value of TF0P Counter, or the peak value of the counter, depending on CMPCMD in register 08h. |
| 0Bh | R | TF0NCOUNT | 7:5 | RSVD | 000 | Reserved. |
| | | | 4:0 | TF0NCOUNT | 00000 | This is either the current value of TF0N Counter, or the peak value of the counter, depending on CMPCMD in register 08h. |
| 0Ch | R | TF1PCOUNT | 7:5 | RSVD | 000 | Reserved. |
| | | | 4:0 | TF1PCOUNT | 00000 | This is either the current value of TF1P Counter, or the peak value of the counter, depending on CMPCMD in register 08h. |
| 0Dh | R | TF1NCOUNT | 7:5 | RSVD | 000 | Reserved. |
| | | | 4:0 | TF1NCOUNT | 00000 | This is either the current value of TF1N Counter, or the peak value of the counter, depending on CMPCMD in register 08h. |

REVISION HISTORY

| Changes from Revision H (April 2013) to Revision I | Page |
|--|--------------------|
| • Changed layout of National Data Sheet to TI format | 15 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| LMH0307GR/NOPB | ACTIVE | csBGA | NYA | 25 | 1000 | Green (RoHS & no Sb/Br) | CU SNAGCU | Level-1-260C-UNLIM | -40 to 85 | 307G | Samples |
| LMH0307GRE/NOPB | ACTIVE | csBGA | NYA | 25 | 250 | Green (RoHS & no Sb/Br) | CU SNAGCU | Level-1-260C-UNLIM | -40 to 85 | 307G | Samples |
| LMH0307GRX/NOPB | ACTIVE | csBGA | NYA | 25 | 3500 | Green (RoHS & no Sb/Br) | CU SNAGCU | Level-1-260C-UNLIM | -40 to 85 | 307G | Samples |
| LMH0307SQ/NOPB | ACTIVE | WQFN | RUM | 16 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 85 | L0307 | Samples |
| LMH0307SQE/NOPB | ACTIVE | WQFN | RUM | 16 | 250 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 85 | L0307 | Samples |
| LMH0307SQX/NOPB | ACTIVE | WQFN | RUM | 16 | 4500 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 85 | L0307 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

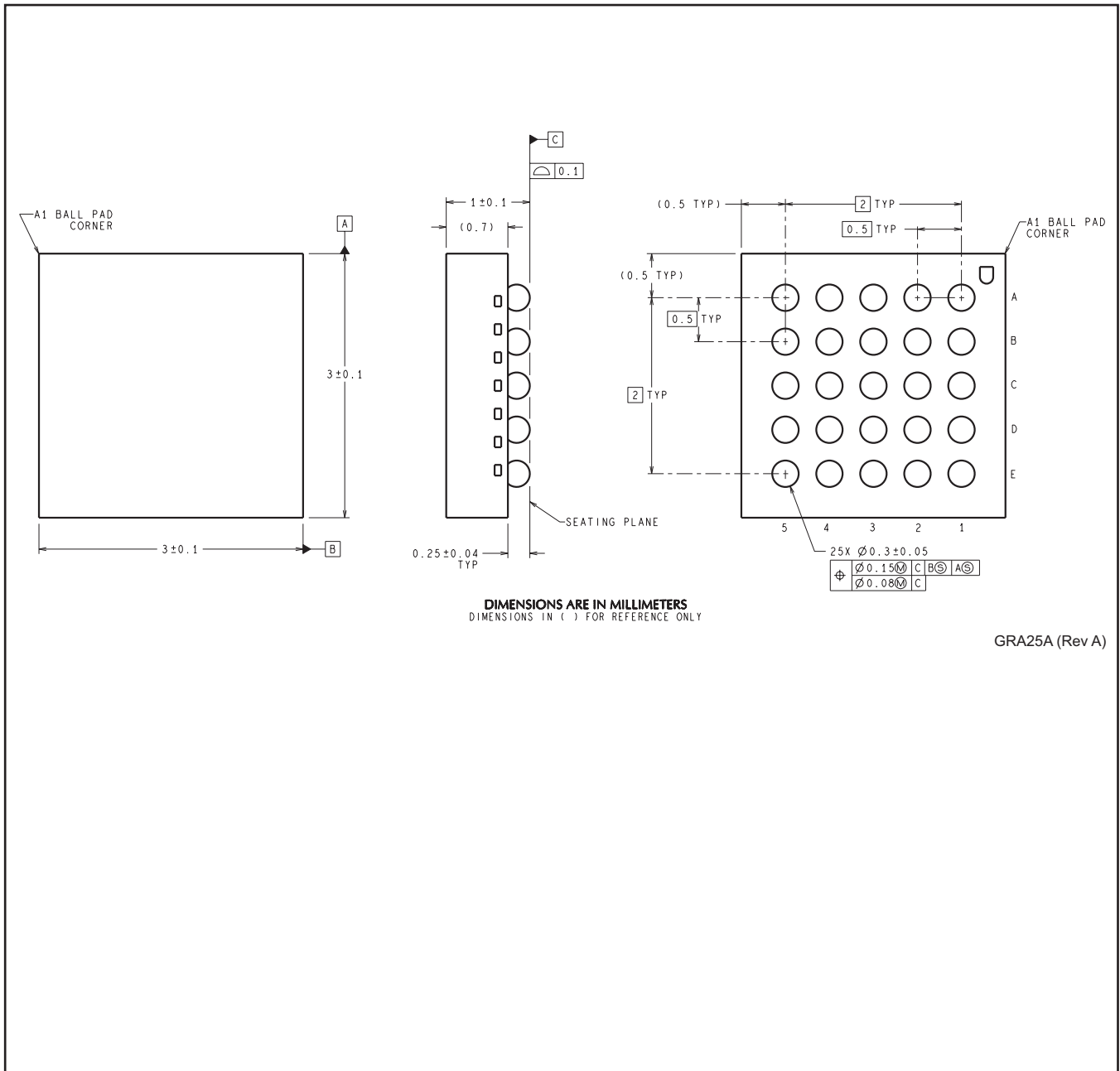
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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GRA25A (Rev A)

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